

1 1. A method comprising:
2 determining whether a register has been updated;
3 and
4 if the register is updated, setting an indicator
5 bit.

1 2. The method of claim 1 including determining
2 whether the register has been updated by checking an
3 indicator bit.

1 3. The method of claim 2 wherein if the register has
2 not been updated, refraining from transferring the contents
3 of the register back to a memory.

1 4. The method of claim 2 including determining
2 whether the register has been updated and if so, saving the
3 contents of the register to memory.

1 5. The method of claim 4 including saving the
2 register contents to memory on a context change.

1 6. The method of claim 1 including assigning a
2 single indicator bit to a plurality of registers.

1 7. An article comprising a medium storing
2 instructions that enable a processor-based system to:

3 determine whether a register has been updated;
4 and
5 if the register is updated, set an indicator bit.

1 8. The article of claim 7 further storing
2 instructions that enable the processor-based system to
3 determine whether the register has been updated by checking
4 an indicator bit.

1 9. The article of claim 8 further storing
2 instructions that enable the processor-based system to
3 refrain from transferring the contents of the register back
4 to a memory if the register has not been updated.

1 10. The article of claim 8 further storing
2 instructions that enable the processor-based system to
3 determine whether the register has been updated and if so,
4 save the contents of the register to memory.

1 11. The article of claim 10 further storing
2 instructions that enable the processor-based system to save
3 the register contents to memory on a context change.

1 12. The article of claim 10 further storing
2 instructions that enable the processor-based system to save

3 the contents of a plurality of registers to memory if an
4 indicator bit is set.

1 13. A processor comprising:
2 a register; and
3 a storage storing instructions to determine
4 whether a register has been updated and if the register is
5 updated, set an indicator bit.

1 14. The processor of claim 13 wherein said storage
2 stores instructions that enable the processor to determine
3 whether the register has been updated by checking an
4 indicator bit.

1 15. The processor of claim 14 wherein said storage
2 stores instructions that enable the processor to refrain
3 from transferring the contents of the register back to a
4 memory.

1 16. The processor of claim 14 wherein said storage
2 stores instructions that enable the processor to determine
3 whether the register has been updated and if so, save the
4 contents of the register to memory.

1 17. The processor of claim 16 wherein said storage
2 stores instructions that enable the processor to save the
3 register contents to memory on a context change.

1 18. The processor of claim 13 including a storage to
2 store said bit.

1 19. A system comprising:
2 a processor;
3 a register coupled to said processor; and
4 a storage storing instructions to determine
5 whether a register has been updated and if the register is
6 updated, set an indicator bit.

1 20. The system of claim 19 including a memory and an
2 interface between said memory and said processor.

1 21. The system of claim 20 wherein said storage
2 stores instructions that enable the processor to determine
3 whether the register has been updated by checking an
4 indicator bit.

1 22. The system of claim 21 wherein said storage
2 stores instructions that enable the processor to refrain
3 from transferring the contents of the register back to the
4 memory.

1 23. The system of claim 21 wherein said storage
2 stores instructions that enable the processor to determine
3 whether the register has been updated and if so, save the
4 contents of the register to the memory.

1 24. The system of claim 23 wherein said storage
2 stores instructions that enable the processor to save the
3 register contents to memory on a context change.

1 25. The system of claim 19 including a storage to
2 store said bit.

1 26. The system of claim 19 including a control
2 register storing said bit and wherein said storage storing
3 instructions and control register are part of said
4 processor.

1 27. The system of claim 19 including a plurality of
2 registers coupled to said processor and a single indicator
3 bit for all of those registers.